SESSION 2 – TAPA I
Advanced CMOS Technology

Tuesday, June 15, 10:20 a.m.
Chairpersons: S. Venkatesan, Motorola
S. Chung, National Chiao Tung Univ.

2.1 — 10:20 a.m.

45nm Node Planar-SOI Technology with 0.296μm² 6T-SRAM Cell, F.-L. Yang, Che.-C. Huang, Chi.-C. Huang, T.-X. Chung, H.-Y. Chen, C.-Y. Chang, H.-W. Chen, D.-H. Lee, S.-D. Liu, K.-H. Chen, C.-K. Wen, S.-M. Cheng, C.-T. Yang, L.-W. Kung, C.-L. Lee, Y.-J. Chou, F.-J. Liang, L.-H. Shiu, J.-W. You, K.-C. Shu, B.-C. Chang, J.-J. Shin, C.-K. Chen, T.-S. Gau, P.-W. Wang, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, S.K.-H. Fung, C.H. Diaz, C.-M. Wu, Y.-C. See, B.J. Lin, M.-S. Liang, J.Y.-C. Sun and C. Hu, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, ROC

The first 45nm node planar-SOI technology has been developed with 6T-SRAM cellof 0.296um2. An adequate static noise margin of 120mV is obtained even at 0.6V operation. Fine patterning with line pitch of 130nm and contact pitch of 140nm by optical lithography is demonstrated. Transistors with 30nm gate length and 27nm slim spacer operate at 1V/0.85V with excellent drive currents of 1000/740and 530/420 uA/um for N-FET and P-FET, respectively. The P-FET current is the best reported so far.

2.2 — 10:45 a.m.

Low Cost 65nm CMOS Platform for Low Power & General Purpose Applications, F. Arnaud, B. Duriez*, B. Tavel*, L. Pain***, J. Todeschini*, M. Jurdit***, Y. Laplanche, F. Boeuf, F. Salvetti*, D. Lenoble, J.P. Reynard, F. Wacquant, P. Morin, N. Emonet, D. Barge*, M. Bidaud*, D. Ceccarelli, P. Vannier, Y. Loquet, H. Leninger, F. Judong, C. Perrot, I. Guilmeau***, R. Palla, A. Beverina, V. DeJonghe*, M. Broekaart*, V. Vachellerie, R.A. Bianchi, B. Borot, T. Devoivre, N. Bicaïs, D. Roy, M. Denais, K. Rochereau*, R. Difrenza, N. Planes, H. Brut, L. Vishnobulta**, D. Reber**, P. Stolk* and M. Woo**, STMicroelectronics, Crolles, France, *Philips Semiconductors, **Motorola, Inc., ***CEA-LETI, France

General Purpose and Low Power 0.5μm² 6T-SRAM bit-cell was developed for 65nmCMOS platform using low cost CMOS process flow. Fully functional bit-cells show 240mV SNM and 35μA cell current at 1.2V operation. GP Ion measured 875μA/μm and400μA/μm for NMOS and PMOS respectively for Vdd=1V. Analog mixed signal transistor parameters show Vt matching (Avt=2.2mV.μm) and analog voltage gain factor (Gm/Gd>2000 for L=10μm). NBTI criteria at 125 C were achieved.

2.3 — 11:10 a.m.

45nm CMOS Platform Technology (CMOS6) with High Density Embedded Memories, M. Iwai, A. Oishi, T. Sanuki, Y. Takegawa, T. Komoda, Y. Morimasa, K. Ishimaru, M. Takayanagi, K. Eguchi, D. Matsushita, K. Muraoka, K. Sunouchi and T. Noguchi, Toshiba Corp., Yokohama, Japan

This paper describes the first 45nm Node CMOS technology (CMOS6) with optimized Vdd, EOT and BEOL parameters. For this technology to be applicable from high performance CPU to mobile applications, three sets of core devices are presented which are compatible with 0.069um2 trench capacitor DRAM and 0.247um2 6Tr.SRAM embedded memories.

2.4 — 11:35 a.m.

Transistor Optimization for Leakage Power Management in a 65nm CMOS Technology for Wireless and Mobile Applications, S. Zhao, A. Chatterjee, S. Tang, J. Yoon, S. Crank, H. Bu, T. Houston, K. Sadra, A. Jain, Y. Wang, D. Redwine, Y. Chen, S. Siddiqui, G. Zhang, T. Laaksonen, C. Hall, S. Chang, L. Olsen, T. Riley, C. Meek, I. Hossain, J. Rosal, A. Tsao, J. Wu and D. Scott, Texas Instruments, Inc., Dallas, TX

A novel transistor optimization strategy that supports the data retention mode of an SRAM is applied to a 65 nm low-power technology with cell area <0.5 um2. It is shown that reducing GDL is critical to achieve 2pA/bit retention leakage current in the SRAM. Process optimizations for 20X GDL reduction and high Idn/Idp of 550/300 uA/um were demonstrated.